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Micropower Precision CMOS Operational Amplifier

Preliminary Technical Data

AD8500

FEATURES

Supply current: 1 µA maximum
Offset voltage: 1 mV maximum
Single-supply or dual-supply operation
Rail-to-rail input and output
No phase reversal
Unity gain stable

PIN CONFIGURATION

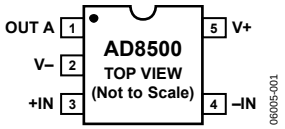

Figure 1. 5-Lead SC70

APPLICATIONS

Portable equipment
Remote sensors
Low power filters
Threshold detectors
Current sensing

GENERAL DESCRIPTION

The AD8500 is a low power, precision CMOS op amp featuring a maximum supply current of 1 µA. The AD8500 has a maximum offset voltage of 1 mV and a typical input bias current of 1 pA, and it operates rail-to-rail on both the input and output. The AD8500 can operate from a single-supply voltage of +1.8 V to +5.5 V or a dual-supply voltage of ±0.9 V to ±2.75 V.

With its low power consumption, low input bias current, and rail-to-rail input and output, the AD8500 is ideally suited for a variety of battery-powered portable applications. Potential applications include ECGs, pulse monitors, glucose meters, smoke and fire detectors, vibration monitors, and backup battery sensors.

The ability to swing rail-to-rail at both the input and output helps maximize dynamic range and signal-to-noise ratio in systems that operate at very low voltages. The low offset voltage allows the AD8500 to be used in systems with high gain without having excessively large output offset errors, and it provides high accuracy without the need for system calibration.

The AD8500 is fully specified over the industrial temperature range (−40°C to +85°C) and is operational over the extended industrial temperature range (−40°C to +125°C). It is available in a 5-lead, SC70 surface-mount package.

Rev. PrA
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REVISION HISTORY

3/06—PrA: Initial Version

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

@ V_S = +5V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	0 V < V_{CM} < +5 V		0.235	1	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +85°C		3	10	µV/°C
Input Voltage Range			−0.3		+5.3	V
Input Bias Current	I_B			1	10	pA
		−40°C < T_A < +85°C			100	pA
		−40°C < T_A < +125°C			600	pA
Input Offset Current	I_{OS}			0.5	5	pA
		−40°C < T_A < +85°C			50	pA
		−40°C < T_A < +125°C			100	pA
Common-Mode Rejection Ratio	CMRR	0 V < V_{CM} < 5 V	75	90		dB
		−40°C < T_A < +85°C	70	90		dB
Large Signal Voltage Gain	A_{VO}	0.1 V < V_{OUT} < 4.9 V	98	120		dB
		0.1 V < V_{OUT} < 4.9 V; −40°C < T_A < +85°C	80			dB
Input Capacitance	C_{DIFF}			TBD		pF
	C_{CM}			TBD		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_{Load} = 100 kΩ to GND	4.970	4.995		V
		R_{Load} = 10 kΩ to GND	4.900	4.960		V
Output Voltage Low	V_{OL}	R_{Load} = 100 kΩ to V_S		0.85	5	mV
		R_{Load} = 10 kΩ to V_S		6.5	15	mV
Short-Circuit Current	I_{SC}	V_{OUT} = GND		±TBD		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	1.8 V < V_S < 5 V	90	110		dB
		−40°C < T_A < +85°C	80			dB
Supply Current/Amplifier	I_{SY}	V_O = V_S/2		0.75	1	µA
		−40°C < T_A < +85°C			1.5	µA
		−40°C < T_A < +125°C			2	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR			0.004		V/µs
Gain Bandwidth Product	GBP			7		kHz
Phase Margin	$Ø_O$			60		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise		0.1 Hz to 10 Hz		6		µVp-p
Voltage Noise Density	e_n	f = 1 kHz		190		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		TBD		fA/√Hz

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@ V_S = +1.8V, V_{CM} = V_S/2, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	0 V < V_{CM} < +1.8 V		0.235	1	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +85°C		3.5	12	µV/°C
Input Voltage Range			−0.3		+1.8	V
Input Bias Current	I_B			1	10	pA
		−40°C < T_A < +85°C			100	pA
		−40°C < T_A < +125°C			600	pA
Input Offset Current	I_{OS}			0.5	5	pA
		−40°C < T_A < +85°C			50	pA
		−40°C < T_A < +125°C			100	pA
Common-Mode Rejection Ratio	CMRR	0 V < V_{CM} < 1.8 V	65	85		dB
		−40°C < T_A < +85°C	60	83		dB
Large Signal Voltage Gain	A_{VO}	0.1 V < V_{OUT} < 1.7 V	88	115		dB
		0.1 V < V_{OUT} < 1.7 V; −40°C < T_A < +85°C	70			dB
Input Capacitance	C_{DIFF}			TBD		pF
	C_{CM}			TBD		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_{Load} = 100 kΩ to GND	1.790	1.798		V
		R_{Load} = 10 kΩ to GND	1.760	1.783		V
Output Voltage Low	V_{OL}	R_{Load} = 100 kΩ to V_S		0.70	5	mV
		R_{Load} = 10 kΩ to V_S		5	15	mV
Short-Circuit Current	I_{SC}			±TBD		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	1.8 V < V_S < 5 V	90	110		dB
		−40°C < T_A < +85°C	80			dB
Supply Current/Amplifier	I_{SY}	V_O = V_S/2		0.65	1	µA
		−40°C < T_A < +85°C			1.5	µA
		−40°C < T_A < +125°C			2	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR			0.004		V/µs
Gain Bandwidth Product	GBP			7		kHz
Phase Margin	$Ø_O$			60		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise		0.1 Hz to 10 Hz		6		µVp-p
Voltage Noise Density	e_n	f = 1 kHz		190		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		TBD		fA/√Hz

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ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	V_{SS} − 0.4 V to V_{DD} + 0.4 V
Differential Input Voltage	±6 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply at 25°C, unless otherwise noted.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Characteristics

Package Type	θ_{JA}	θ_{JC}	Unit
5-Lead SC70 (KS-5)	376	126	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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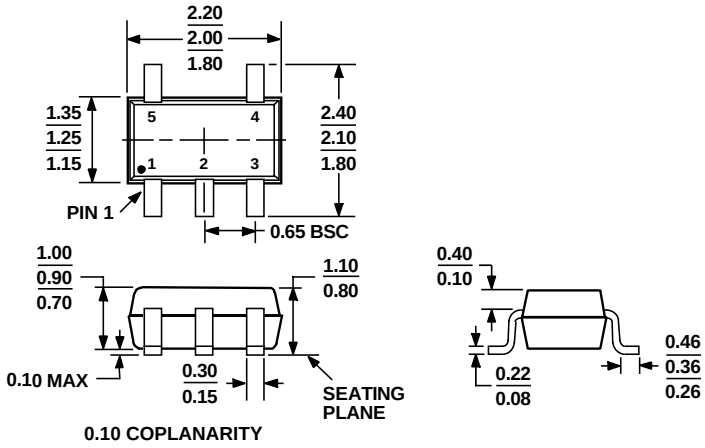
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-203-AA

Figure 2. 5-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8500AKSZ-R2[1]	−40°C to +125°C	5-Lead SC70	KS-5	A0F
AD8500AKSZ-REEL[1]	−40°C to +125°C	5-Lead SC70	KS-5	A0F
AD8500AKSZ-REEL7[1]	−40°C to +125°C	5-Lead SC70	KS-5	A0F

[1] Z = Pb-free part.

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